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L3	52284	(dynam$5 ramdom$4 vary variable differen$4) with ((block data frame) near3 (size quantity volume length width))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/03/31 11:32
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L5	388	multiplex$4 same 4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/03/31 11:37
L6	30	(((head front) with (FIFO input$4 output$4)) same ((tail end back) with (FIFO input$4 output$4))) and 5	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/03/31 11:37
L7	1729	multiplex$4 and 4	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/03/31 11:37
L8	98	(((head front) with (FIFO input$4 output$4)) same ((tail end back) with (FIFO input$4 output$4))) and 7	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/03/31 11:37

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1 Interactive global illumination in dynamic scenes

Parag Tole, Fabio Pellacini, Bruce Walter, Donald P. Greenberg

July 2002 **ACM Transactions on Graphics (TOG) , Proceedings of the 29th annual conference on Computer graphics and interactive techniques**, Volume 21 Issue 3

Full text available: pdf(13.82 MB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we present a system for interactive computation of global illumination in dynamic scenes. Our system uses a novel scheme for caching the results of a high quality pixel-based renderer such as a bidirectional path tracer. The Shading Cache is an object-space hierarchical subdivision mesh with lazily computed shading values at its vertices. A high frame rate display is generated from the Shading Cache using hardware-based interpolation and texture mapping. An image space sampling sc ...

Keywords: Monte Carlo techniques, illumination, parallel computing, ray tracing, rendering, rendering systems

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Handshake-wave combined approach with runtime reconfiguration for designing a low latency asynchronous FIFO

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Abstract
In this paper, a novel design scheme combining a handshake protocol and wave pipeline is proposed to improve latency performance of an asynchronc linear FIFO. The stage control of the proposed FIFO can be reconfigured dynamically to be one of two different operating styles, waving or handshakin according to the status of data flow in the FIFO. The use of wave pipelining in a control and a datapath can eliminate delays of handshaking circuits anc latching data respectively. The proposed circuits have been designed with 0.25 /spl mu/m, 2.5 V CMOS process technology and simulated using HSPIC Preliminary results show about two times improvement on latency performance over a state-of-art linear FIFO circuit while retaining throughput and a simple linear structure.

Index Terms
Inspec
Controlled Indexing
CMOS logic circuits SPICE asynchronous circuits flip-flops logic CAD pipeline processing

Non-controlled Indexing
CMOS process technology FIFO design HSPICE asynchronous linear FIFO baseline control structure handshake-wave combined approach latch control latency performance low latency asynchronous FIFO runtime reconfiguration stage control wave pipelining
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References

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